

**INTEGRATED CIRCUIT WITH TEST PAD STRUCTURE AND**  
**METHOD OF TESTING**

**ABSTRACT OF THE DISCLOSURE**

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A semiconductor device has a large number of bond pads on the periphery for wirebonding. The semiconductor device has a module as well as other circuitry, but the module takes significantly longer to test than the other circuitry. A relatively small number of the bond pads, the  
10 module bond pads, are required for the module testing due, at least in part, to the semiconductor device having a built-in self-test (BIST) circuitry. The functionality of these module bond pads is duplicated on the top surface of and in the interior of the semiconductor device with module test pads that are significantly larger than the bond pads on the  
15 periphery. Having large pads for testing allows longer probe needles, thus increasing parallel testing capability. Duplicating the functionality is achieved through a test pad interface so that the module bond pads and the module test pads do not have to be shorted together.

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